Notice of Allowability	Application No. 10/677,629	Applicant(s) PHONG ET AL.	
	Examiner Joni Hsu	Art Unit 2671	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *papers received May 3, 2005*.

2. ☒ The allowed claim(s) is/are *1-25*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Response to Amendment

2. The Examiner acknowledges that the address of each inventor is listed in the ADS, and therefore the objection to the declaration is withdrawn.

In light of Applicant's amendment to the abstract, the objection to the abstract is withdrawn.

In light of Applicant's amendment to include "we claim" to the heading of the claims, the objection to the specification is withdrawn.

In light of Applicant's amendment to renumber the second claim 14 and claim 15, the objection to the claims is withdrawn.

3. Applicant's arguments, see pages 11-14, filed May 3, 2005, with respect to Claims 1-25 have been fully considered and are persuasive. The rejections under 35 U.S.C. 103(a) of Claims 1-15 have been withdrawn.

Allowable Subject Matter

4. Claim 1-25 allowed.

The following is an examiner's statement of reasons for allowance:

5. The prior art singly or in combination do not teach or suggest a cache memory system for use in a motion estimation system, comprising a first cache memory defined in terms of a first width and a first height, and a second cache memory defined in terms of a second width and a second height, wherein the second height is less than the first height; the cache memory system being structured in one of two arrangements: a first arrangement having banks of memory from the second cache memory concatenated vertically such that their concatenated height is at least equal to the first height, and the concatenated banks being arranged to be appended to the width of the first cache memory to form a single contiguous address space, and a second arrangement having banks of memory from the first and second caches stacked vertically, and arranged to be addressed as two separate address spaces, as recited in Claims 1, 6, 10, 20, and 22. Claims 2-5, 7-9, 11-19, 21, and 23-25 rely upon these claims, and therefore also contain allowable subject matter.

6. The closest prior art (Herluison US005696698A) teaches a cache memory system for use in a motion estimation system (Col. 1, lines 8-13), comprising: a first cache memory (2, Figure 1) defined in terms of a first width (m) and a first height (n) (Col. 4, lines 17-19), and a second cache memory (1) defined in terms of a second width (m/2) and a second height (n), wherein the second width is less than the first width (Col. 4, lines 28-32); an arrangement having blocks of

memory from the second cache memory concatenated horizontally (Col. 4, lines 45-49) such that their concatenated width is at least equal to the first width (Col. 4, lines 10-39), as shown in Figure 1. Figure 1 shows that the blocks of memory from the first and second caches are stacked horizontally, but Herluison describes that they are also stacked vertically (Col. 4, lines 45-49). If they are stacked vertically, then the width becomes the height and the height becomes the width. In that case, the second height is less than the first height. Since the blocks are also stacked vertically, Herluison describes an arrangement having blocks of memory from the first and second caches stacked vertically, and arranged to be addressed as two separate address spaces (Col. 3, lines 17-27). However, Herluison does not teach banks in the second cache, the banks of memory from the first and second caches are stacked together vertically, and in the first arrangement, the concatenated banks of the second cache memory are arranged to be appended to the width of the first cache memory to form a single contiguous address space.

7. Another prior art (Kim US006342895B1) teaches a system for motion compensation (Col. 2, lines 1-4) with two memory banks (Col. 4, lines 2-6), and the set of macro block sets are constructed in the vertical direction (Col. 3, lines 57-59). The macro block data is stored in the same row, and the data is read and output continuously because the consecutive data are in different banks (Col. 4, lines 6-8). Therefore, Kim teaches that blocks of memory in the first and second bank are concatenated vertically, and the second bank is appended to the width of the first bank to form a single contiguous address space. However, Kim does not teach that the banks of memory are stacked vertically and a second arrangement having banks of memory from

the first and second caches stacked vertically, and arranged to be addressed as two separate address spaces.

8. Another prior art (Ju US006753871B2) teaches a memory access method for overlapping partial boundary data in order to reduce or eliminate cross-page penalties when reading data (Col. 1, lines 63-66). By the overlapping boundary data technique, when the system detects that the prediction block A will run cross the vertical boundary of page M, the system will read out the data of the prediction block A from page N, and because the prediction block A is entirely enclosed by page N, no page crossing results. Therefore, the pages M and N can be treated as a whole virtual page M_N (Col. 2, lines 55-62). According to Applicant's disclosure, the two caches are regarded as being concatenated logically or virtually (page 6, lines 23-25). However, Ju does not have the same memory arrangement as claimed in this application.

9. Another prior art (Vainsencher US006005624A) teaches that the reference frame memory map or search area is such that a top field resides in a first bank A and a bottom field resides in a second bank B (Col. 10, lines 31-35). Since fields reside in different banks and motion vectors are the same for both fields, the page crossings occur in the same location for each respective bank or field, and this the number of page misses is not doubled (Col. 10, lines 48-52). Therefore, this method minimizes the maximum number of page crossing required in retrieving this data from the memory (Col. 4, lines 43-48). However, Vainsencher does not have the same memory arrangement as claimed in this application.

10. Another prior art (Murdock US006222883B1) teaches a method of increasing the search range for motion estimation without increasing the storage capacity or processing time (Col. 3, lines 40-46) by defining from a reference frame a diamond-shaped search window about a current position of the macroblock; partitioning the diamond-shaped search window into multiple search regions and reassembling the multiple search regions into a rectangular search area; and using the rectangular search area to search within the diamond-shaped search window for a best matching reference macroblock for the current macroblock (Col. 3, lines 36-60). This method minimizes the total size of a memory which can be used for storing search areas without increasing the processing time (Col. 3, lines 40-46), which is the same advantage as Applicant discusses in the disclosure of this application (page 9, lines 4-11). However, Murdock does not have the same memory arrangement as claimed in this application.

11. Another prior art (Khan US006553552B1) teaches a re-configurable memory that uses a plurality of memory banks, and can be reconfigurable in such a way as to be optimized for different applications (Col. 1, lines 44-50). Applicant's invention is also for a re-configurable cache to optimize the overall size of the cache memory to support different applications (page 6, lines 1-3). However, Khan is not for a cache memory system for use in a motion estimation system.

12. Another prior art (Ewoldt US 20020103977A1) teaches a cache memory system with banks of memory stacked vertically [0021]. However, Ewoldt is not for a cache memory system for use in a motion estimation system.

13. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Prior Art of Record

The following prior art not relied upon is considered pertinent to applicant's invention.

1. Herluison (US005696698A) teaches the use of cache memories to form motion estimations of picture portions, a current picture portion being compared with its environment in a preceding picture (Col. 1, lines 8-13).

2. Kim (US006342895B teaches a memory allocation method for storing/reading the decoded data in block sets in/from a memory by grouping the data blocks into sets of blocks and storing the block sets in the memory in block sets (Col. 2, lines 51-56).

3. Ju (US006753871B2) teaches a memory access method of a video decoding system that utilizes a method of overlapping boundary data to reduce cross-page penalties when reading data (Col. 1, lines 7-11).

4. Vainsencher (US006005624A) teaches a MPEG decoder system for performing motion compensation which stores macroblocks in a skewed tile arrangement to reduce page crossings during block accesses and thus provide improved performance (Col. 1, lines 14-20).

5. Murdock (US006222883B1) teaches an encoder with an enhanced search range for motion estimation and compensation, without adversely impacting chip performance or design criteria (Col. 1, lines 6-19).

6. Khan (US006553552B1) teaches a re-configurable memory that uses a plurality of memory banks, and can be reconfigurable in such a way as to be optimized for different applications (Col. 1, lines 44-50).

7. Ewolt (US 20020103977A1) teaches a cache memory system with banks of memory stacked vertically [0021].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joni Hsu whose telephone number is 571-272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on 571-272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JH

Kee M. Tung
Primary Examiner